



### Volume 26 Number 1

**Summer 2020** 

# eXpress Version 7.3 — Join the MBSE Party!!

With the release of *eXpress* version 7.3, existing *eXpress* models can be used to perform Sneak Path Analysis—yet another addition to the growing list of tasks you can accomplish using a single set of models in *eXpress*.

Each time that DSI expands into a new discipline—testability analysis, diagnostic development, reliability assessment, fault tree analysis, prognostic evaluation, maintenance trade studies, sneak path analysis—the value of creating models in *eXpress* grows not proportionally, but exponentially.



With single-purpose tools, engineering is a lonely endeavor.

Not only are you able to use **eXpress** models for multiple tasks in multiple disciplines, but you are also able to incorporate the information learned from one discipline into analyses that are normally treated as independent endeavors.

For instance, the Critical Failure Diagnosis chart in FMECA Plus helps analysts identify areas where system diagnostics are not sufficiently robust to support *operational* (as opposed to *logistic*) goals—an activity that is not a standard part of either testability or FMECA analysis.

1
2-3
4
4

*eXpress* data is applied during Fault Tree Analysis to determine the risk associated with sub-optimal diagnostics. Risk is usually not considered during diagnostic development and the Risk & Safety folks rarely, if ever, take actual diagnostics into account.

In addition to sneak paths, **eXpress** can identify areas where system failures, combined with sneak conditions, can result in potentially disastrous outcomes. Fault Tree Analysis—which evaluates the impact of different failure combinations—usually avoids having sneaky guests on its invite list.



Use eXpress and all your colleagues will want to join the party.

With all the excitement in the air about collaborative engineering, don't be satisfied with a field of single-purpose wallflowers. Invite *eXpress* to be the life of your MBSE party—you'll be surprised at the heights your team can reach.

### Keep In the Know

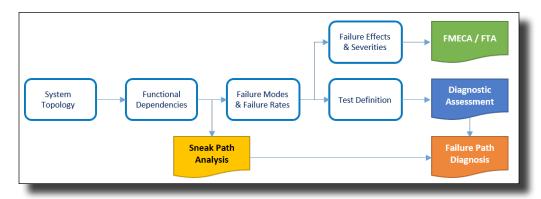
- New Feature: Sneak Path Analysis Module
- Interoperability: TCP/IP Support in DSI Workbench
- Game Changer: Tablet-Based Diagnostics
- Coming up: Extensive Online Training

Latest Softw	bench 5.0 9/20			
eXpress	7.3	7/20		
Run-Time Authoring To	ol 5.5.7	10/19		
DSI Workbench	5.0	9/20		
• STAGE	Act II. Scene 3	10/16		

# Sneak Path Analysis Using eXpress

The new *eXpress* Sneak Path Analysis module allows sneak circuit analysis to be performed using the same hierarchical models that you've created for diagnostic and reliability engineering efforts in *eXpress*.

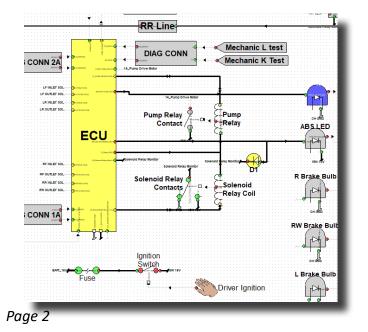
In addition to sneak path analysis, this module can also identify situations in which crosstalk or failures (alone, or in combination with other failures) result in undesired signal paths. It can then determine the probability that a critical failure path will occur (in a manner similar to the probabilities of failure that appear in a Fault Tree Analysis) and the likelihood that the failures leading up to a critical path will be prognosed, detected and/or diagnosed using the diagnostic strategies developed in *eXpress*.

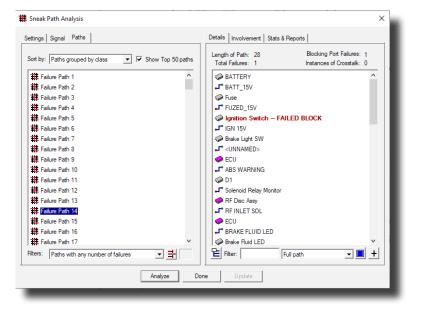


Sneak Path Analysis can be performed early in the modeling process—long before reliability and test data have been added. Sneak, failure and crosstalk paths can therefore be identified at a point when this knowledge can still be used to improve the design. Later, after diagnostics have been developed, you can determine the likelihood of failure paths occurring and see how well they can be prognosed and/or diagnosed.

The hub of the module is the Sneak Path Analysis dialog, which allows you to determine, examine and analyze sneak, crosstalk and/or failure paths within a hierarchical system modeled in *eXpress*.

In the example at right, the analysis uncovered no sneak paths. It did, however, identify a number of cases where one or more failures—analyzed in conjunction with possible sneak conditions (such as reverse signal flow or input-toinput shorts)—could result in a critical path that would not be identified as a sneak path. Because design activities that examine the impact of different failure combinations (such as FMECA & Fault Tree Analysis) do not take sneak conditions into account, this analysis can uncover high-risk areas of the design that might otherwise go undetected.





When a sneak, crosstalk or failure path is selected on this dialog, objects are color-coded in the main design window, allowing the analyst to easily review the path.

For instance, the analyst can easily identify by their colors those objects through which signals flow in reverse (yellow) and objects that must fail for a critical path to occur (red). Existing approaches to sneak circuit analysis involve a specialized inspection of schematic data in which topology is simplified into "node topographs" and then examined for patterns known to contribute to sneak conditions. Although this approach may be effective when analyzing simple switching circuitry, the task becomes considerably more difficult when the topological conditions for a sneak path exist within complex parts (and therefore cannot be identified from connectivity alone) or are distributed across multiple levels of a large system (crossing between and/or descending within multiple schematics).

Fortunately, **eXpress** models—because they gather together multiple levels of system topology into a single hierarchical model and represent not only how signals flow *between* components, but also how signals flow *through* components—are ready made for sneak analysis. Moreover, the **eXpress** Sneak Path Analysis module has been designed with large-scale designs in mind. Analysis can be performed randomly (to quickly identify a representative selection of possible undesired paths) or systematically (to identify all sneak, crosstalk, and/or failure paths within the design).

The Involvement panel lists ports and/or nets sorted in an order that helps the analyst examine their relative role in the undesired paths (sneak, crosstalk and failure) that have been identified for a given signal. By default, the panel lists all ports and nets that participate in at least one undesired path—the number of occurrences (paths) is appended to the name.

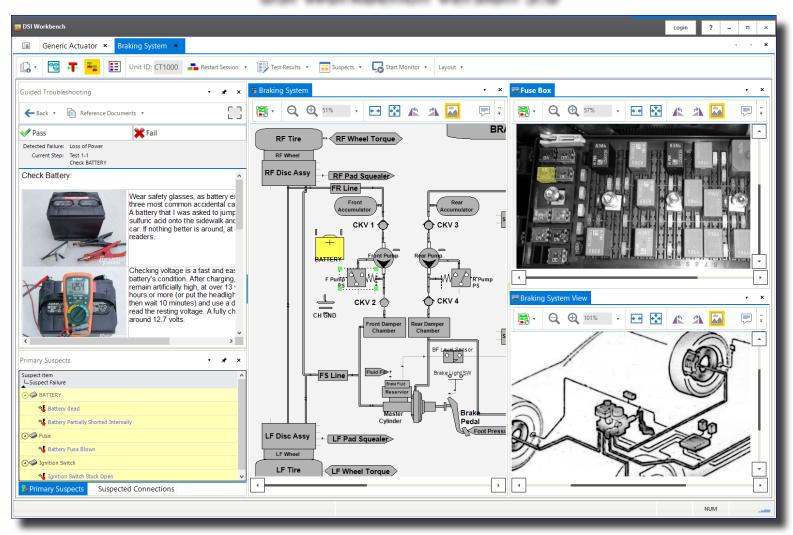
This list can be sorted in different orders to help the analyst discover the ports through which the signal travels most frequently in reverse, or the ports that—when they fail—contribute to the greatest number of failure paths. This panel is useful both in preliminary analyses (to help identify ports that should not be included in sneak or failure paths) and in final analyses (to help identify areas where design improvements will have the greatest impact).

The Sneak Path Analysis module provides four different reports (portions of which are depicted below): the Path Analysis Details Report, the Path Analysis Involvement Report, the Path Analysis Signal Report and the Failure Path Diagnosis Report. These reports—along with all other aspects of the Sneak Path Analysis module—are described in the white paper "Sneak Path Analysis in *eXpress*", which is available upon request from DSI.

Involvement
All involved ports & nets 🔹 Sort: Occurrences 💌
BATT_15V - 321 occurrences
BATT_15V [BATTERY] 321 occurrences
BATT_15V [Fuse] 321 occurrences
J <sup>●</sup> BRAKE FLUID LED 321 occurrences
BRAKE FLUID LED [Brake Fluid LED] 321 occurrences
<ul> <li>BRAKE FLUID LED [ECU] 321 occurrences</li> </ul>
J <sup>●</sup> FUZED_15V 321 occurrences
<ul> <li>FUZED_15V [Fuse] 321 occurrences</li> </ul>
<ul> <li>FUZED_15V [Ignition Switch] 321 occurrences</li> </ul>
J <sup>●</sup> IGN 15V 321 occurrences
<ul> <li>IGN 15V [Ignition Switch] 321 occurrences</li> </ul>
Solenoid Relay Monitor 310 occurrences
- 1_ECU POWER [ECU] 270 occurrences
29_ABS WARNING LED [ECU] REVERSE FLOW [82/2]
ABS WARNING 217 occurrences
ABS WARNING [D1] REVERSE FLOW [82/217]
Solenoid Relay Monitor ID11 REVERSE FLOW I82/2171
E Filter:

	Path Analysis Details Re	pon	Top 26	5 Involved Ports	& Note			
	Design: sneak1.exd Signal: DOWNSTREAM		TOP 23	J III VOIVEU POILS	& NEIS		Failures /	
	Signal. DOWNS TREAM		Port / Net Name	Entity Type	Occurrences	Reversed	Crosstalk	Pctg
	Summary		[GROUP ORUXA]	net	13	0	6	92.86
			FI	port	12	0	0	85.719
				net	12	0	0	85.719
	Sneak Paths Found: 2 Crosstalk Paths Found: 6			not	0	0	L õ	57.14
	Failure Paths Found: 6						0	57.14
			Path	Details			0	57.14
	Paths Examined: 36 Analysis Method (Status): Systematic (Cor	nnlotod)					0	57.14
	Total Processing Time: 00:00:00	ipieteuj	Sneal	k Path 2				
	· · · · · · · · · · · · · · · · · · ·		Steps (10)	Entity Type	Status		0	57.14
			(A) ut of A IGROUP ORUXA1	output port net	-		0	57.14
			px-in [B]	input port			0	57.14
	Signal Details		x-out [B] net out of B	output port net			0	57.14
	<b>-</b>		d-out [D]	output port	REVER SE FLO		0	57.14
	sneak1.exd		d-in-from-e [D]	input port	REVER SE FLO	WC	0	57.14
	sneak1.exd		net from E to D e-out-to-d [E]	net output port	REVER SE FLO	W	0	50.00
Origins: 2	Reverse Flow on Fail: 0		e-in-from-b [E]	input port	The Ferroe Fe		0	50.00
Endpoints: 2	Reverse Flow Safe: 0	4					0	50.00
Blocking: 0	Cross-Deps on Fail: 2	1	Crossta	alk Path 1			0	42.86
Dioonning.			Steps (7)	Entity Type	Status		0	42.86
	Entities	Entity Type	a-out [A] net out of A [GROUP ORUXA]	output port net			0	42.86
[A]		output por	net out of O [GROUP ORUXA]	net	CROSSTAL	ĸ	0	42.86
<u>[U]</u>		output por	p-in-from-o (P) p (P)	input port output port			0	28.57
from-b [E] from-p [Q]		input port	net out of P	net			4	28.57
rom-a [C]		input port input port	q-in-from-p [Q]	input port			0	28.57
rom-b [C]		input port					0	28.57
UP ORUXA		net		Failure Path 1			0	28.57
	sneak1X.exd		Steps (7)	Entity Type output port	Status		U	20.31
			net out of U [GROUP ORUXA]	net				
Origins: 0			ut of A [G ROUP ORUXA]	net	CROSSTAL	ĸ		
Endpoints: 0	Summary		rom-a [C] from-b [C]	input port input port	FAILED / REVER SI	EFLOW		
Blocking: 1			ut of B	net				
			(rom-b [E]	input port				
+ [¥2]	Probability that Failure Path Occurs	s: 1.000F-06	6					
out [X3]		5. 11000E-00		e Path 1				
	Probability Progno see	d: 38.71	Steps (6)	Entity Type output port	Status			
	Probability Detected	d: 100.00	ut of A [GROUP ORUXA]	net				
	Probability Isolated	d: <b>21.05</b>	rom-a (C) from-b (C)	input port input port	FAILED / REVERS	EFLOW		
			ut of B	net	ALLED / REVERS			
			from-b (E)	input port				

## **DSI Workbench Version 5.0**



DSI Workbench has a brand new GUI — That's right, DSI Workbench has been overhauled with a new look to better support the latest run-time platforms (including computers with high-resolution 4K and touch displays).

Workbench's new project management screen allows multiple diagnostic sessions to execute simultaneously. In addition to importing test results, users can now enter test measurements directly and Workbench will determine if the values indicate a Pass or Fail test result.

Messaging protocols using TCP/IP and windows message queues can be used to control communication to and from DSI Workbench in the test environment. Finally, item status colors can be selectively enabled or disabled for individual "views" using the color legend, allowing the technician to focus on exactly the components of interest.

### New in Version 5.0

- Support for high-resolution (4K) displays
- Redesigned GUI for touch panel displays
- Project management support facilitating the use of multiple diagnostics
- Ability for the user to enter measured values rather than Pass/Fail test results
- Master/Slave control of Workbench using TCP/IP messaging protocols
- View control using color legend

China



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